Application No.: 09/752,123   Docket No.: JCLA6706

<u>In The Claims:</u>

Claim 1. (Canceled)

Claim 2. (Currently Amended) An apparatus for coprocessor data access control, comprising

a central processing unit, for executing central processing unit instructions to perform data processing, wherein the central processing unit instructions includes a plurality of coprocessor memory access instructions;

a memory unit, coupled to the central processing unit, for storing data words; and

a <u>plurality of</u> coprocessor<u>s, each of the coprocessors</u> coupled to the central processing unit and the memory unit, for accessing and processing the data words stored in the memory unit by one of addressing modes under control of the coprocessor memory access instructions executed by the central processing unit, wherein

.the coprocessor memory access instruction having an indicating field, ~~and N data words are accessed to or from the memory unit by the coprocessor according to the value of the indicating field, wherein N is a value greater than or equal to 1.~~

_wherein the indicating field of the coprocessor memory access instruction includes a coprocessor number field, for storing information about a specific coprocessor to be activated, <u>and a coprocessor register field, for storing information about specific registers to be used, and number of word data that needs to be transmitted is determined by the coprocessor number field</u>

Page 2 of 7

and the coprocessor register field, and the coprocessor number field determines one of the coprocessors to be activated.

Claims 3-5. (Canceled)

Claim 6. (Currently Amended) A coprocessor data access control method, comprising the steps of:

providing an instruction having an indicating field; and

accessing ~~N data words to or from~~ a memory unit by a specified coprocessor according to the value in the coprocessor indicating field, ~~wherein N is a value greater than or equal to 1,~~

wherein the indicating field of the coprocessor memory access instruction includes a coprocessor number field, for storing information about a specific coprocessor to be activated, and a coprocessor register field, for storing information about specific registers to be used, and number of word data that needs to be transmitted is determined by the coprocessor number field and the coprocessor register field

wherein, the coprocessor number field determines one of a plurality of coprocessors to be activated .

Claims 7-8. (Canceled)

Claim 9. (Currently Amended) An instruction format recorded on a computer readable medium for a coprocessor data access control, wherein the instruction format includes an indicating field so that while the instruction format is read by the computer, ~~a particular~~

Application No.: 09/752,123   Docket No.: JCLA6706

~~coprocessor being used and~~ the number of data words being accessed to or from a memory unit is

determined by ~~the value of~~ a coprocessor number and a register number specified in the

indicating field only, and the coprocessor number determines one of a plurality of coprocessors to

be activated.

Claim 10. (Original) The instruction format of claim 9, wherein the indicating field of the

instruction format is a coprocessor number field.

Claim 11. (Original) The instruction format of claim 9, wherein the indicating field of the

instruction format is a coprocessor register field.

Claim 12. (Original) The instruction format of claim 9, wherein the indicating field of the

coprocessor memory access instruction includes a coprocessor number field and a coprocessor

register field, wherein coprocessor number field is used for storing information about a specific

coprocessor to be activated, and the coprocessor register field is used for storing information

about specific registers to be used in the data processing.

Page 4 of 7